

A Low-power, CMOS Optical Communication Receiver System for 5Gbps Applications based on RGC Structure

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ABSTRACT:

An optical communication receiver system is presented in this research using 65nm CMOS, which consists of three low-power active differential stages as Limiting Amplifier (LA) following an ultra-low-power RGC-Based Transimpedance Amplifier (RB-TIA). The presented active circuit of the RB-TIA is followed by a gain stage that extends the -3dB frequency of the circuit by creating a resonance for the load capacitance. Thus, needless of consuming extra power, a wide-bandwidth circuit has been designed. In addition, employing active-inductor loads within the LA stages enables obtaining a 5Gbps receiver system. The RB-TIA consumes 573 μ W and provides 3.52GHz frequency, while the complete optical receiver consumes only 4.76mW power to provide -3dB frequency of 3.5GHz and high gain of 80dB (10'000). The circuits have been mathematically presented and discussed, and simulations have justified the presented circuit design.

KEYWORDS: Optical Receiver, Low-Power, Transimpedance Amplifier, Limiting Amplifier, Regulated Cascode.

1. INTRODUCTION

Demands for high-speed systems for various communication applications are growing every year in 21st century. Optical fiber networks and cable communication networks possess a special place in modern Giga-bit-per-second communication systems. One of the important parts of an optical communication system is the optical receiver, while the most important part in an optical receiver system, whose performance affects the complete receiver system, is the Transimpedance Amplifier (TIA) stage [1-2].

Recently, different designs as the transimpedance amplifiers are introduced. Among them, the most popular topologies are as follows: inverter-based TIAs [3], [4], current mirror-based TIAs [5], [6] and above of all, RGC structures, which has attracted many researcher's attention in the last decade [7-8]. One trend in designing TIAs, as in this paper, is to resolve the bottleneck of the -3dB frequency, in which different techniques are used, such as: passive inductive peaking technique [9], the zero pole cancellation [10], a three-dimensional inductor converter [11] and passive shunt peaking technique [12]. Of course, all the above mentioned approaches present some superiorities and some flaws, due to the intrinsic existence of trade-offs among different characteristics. Some of these

techniques such as in [10-12] require to occupy a large area, which is known as a flaw in manufacturing process.

However, the RGC circuit is an interesting structure among researchers, which is commonly used in order to alleviate the effect of parasitic capacitance of the photodiode that massively limits the -3dB frequency [13]. The advantage of using RGC stage in comparison with passive inductive peaking technique is that the RGC stage would extend the frequency bandwidth without using a passive inductor. This obviously yields that the chip area can be saved in RGCs in comparison with passive inductive peaking techniques [14].

For example, in [26] a ladder matching network consisted of three inductors is introduced to eliminate the effect of the dominant pole in an RGC stage. The results exhibit an enhanced bandwidth in cost of larger area. Furthermore, in [27] a simple three stage amplifier is proposed with a proper characteristic of low power, but in cost of high levels of thermal noise.

Here, in the proposed Regulated cascode-Based TIA (RB-TIA) in this manuscript, smaller CMOS technology is utilized, which yields more complicated second order effects. Designing this RB-TIA circuit is done utilizing only one resistor as the feedback network (to save chip area), and two gain stages are used after

the RGC stage to provide extra bandwidth and gain. Moreover, less supply voltage is used to prevent quantum tunneling phenomenon. Furthermore, the conventional inductive peaking technique is now implemented with active elements. Hence, a zero is formed in the transfer function of the RB-TIA, which extends the -3dB frequency and occupies less area on chip in comparison with utilizing passive inductors. By using the trade-offs between the power consumption and this extra -3dB frequency, it is possible to reduce the bandwidth in exchange of reducing the power dissipation of the RB-TIA.

Hence, the organization of this paper is as follows: in section 2, the system structure is discussed. The proposed RB-TIA structure is presented and discussed in section 3. The receiver system is presented in section 4. Section 5, presents the simulation results for the RB-TIA and the optical receiver and finally, conclusion results are given in section 6.

2. THE SYSTEM STRUCTURE

The optical receiver is supposed to convert the produced current of the photodiode to an amplified voltage, which can be logically proper for digital circuits. The gain, bandwidth and input referred noise of a TIA stage mainly affect the performance of the optical receiver.

In Fig. 1, the block diagram of the optical communication receiver system stage is shown. The block diagram in Fig. 1 consists of a RGC stage as the first stage of the TIA with low input resistance followed by a closed loop amplifier to amplify the main signal, a replica TIA, and three stages of differential LAs to eliminate the thermal noise of the TIA stage beside providing extra gain. In next sections, the schematic level of each block in this figure is discussed and the whole front-end system is analyzed.

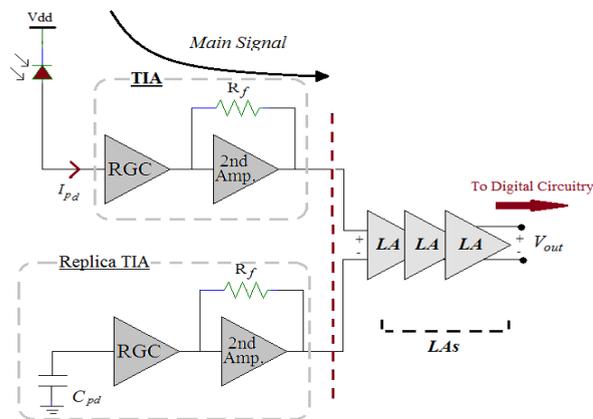


Fig 1. Structure of the proposed optical communication receiver system.

3. THE PROPOSED TIA CIRCUIT

Fig. 2 demonstrates the circuit structure of a conventional RGC stage. The transimpedance gain of this structure and its input resistance can be written as equations (1) and (2).

$$Z_{T,(0)} \approx R_1 \tag{1}$$

$$R_{in(0)} = \frac{1}{\frac{1}{R_{CS}} + g_{m,MN1}(1+A_{CS})} \tag{2}$$

Where, R_{CS} is the equivalent resistance of the current source and A_{CS} is the voltage gain of the common-source stage (booster amplifier), which can be calculated as equation (3).

$$A_{CS} = g_{m,MN2} \cdot R_2 \tag{3}$$

However, in the conventional RGC structures, the value of A_{CS} is limited due to the use of low supply voltage. So, considering equation (4), decreasing the value of R_2 results in an increase in the value of current passing through MN2, which itself increases A_{CS} at the cost of consuming higher power value.

$$I_{D,MN2} = \frac{V_{DD} - V_{gs,MN1} - V_{gs,MN2}}{R_2} \tag{4}$$

Moreover, Fig. 3 demonstrates the proposed modified RB-TIA circuit structure. It consists of an active type of RGC, to present small values of resistance at input node, plus an extra gain stage which itself consists of a common drain structure to compensate the -3dB frequency limitations of the RB-TIA and a common source structure to provide further amplification for the signal. However, the input resistance of the RGC stage can be calculated as equation (4).

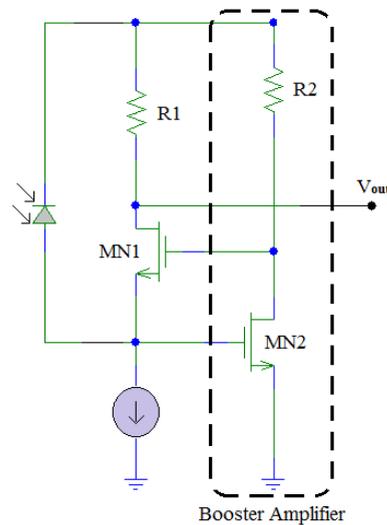


Fig. 2. Circuit structure of a conventional RGC stage.

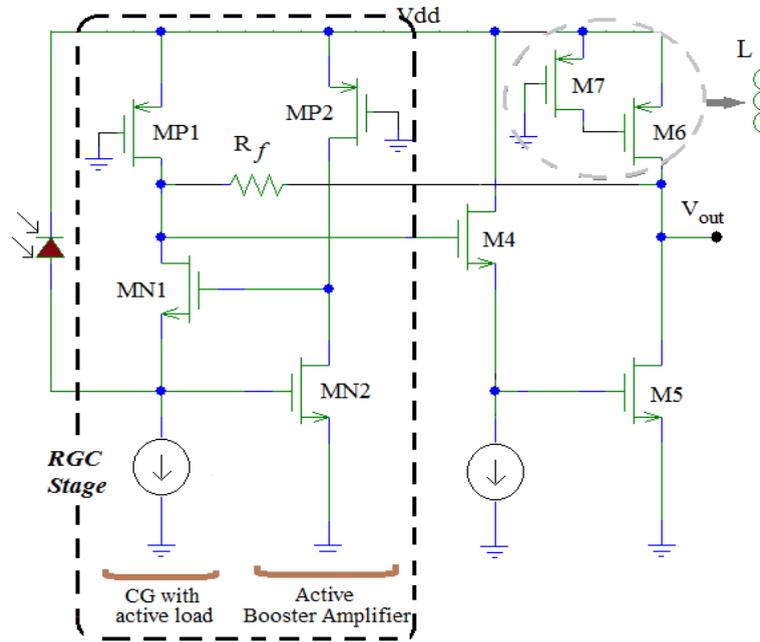


Fig. 3. The Proposed TIA circuit structure.

$$R_{in(0)} = \frac{1}{\frac{1}{R_{CS}} + g_{m,MN1}(1+A_V)} \quad (5)$$

In which the A_V parameter is the gain of the active booster amplifier, calculated as in equation (6).

$$A_V = (g_{m,MN2}) (r_{o,MP2} || r_{o,MN2}) \quad (6)$$

As it is obvious in equation (5), the input resistance of the RB-TIA is reduced by a factor of " $A_V \gg A_{CS}$ ", which results in an extension in the -3dB frequency of the RB-TIA circuit in addition to a higher transimpedance gain value in comparison with conventional RGC structures.

However, the main challenge in design of a high-performance TIA is dealing with the high parasitic capacitance value of the photodiode, which forms the dominant pole at the input node of the RB-TIA circuit. So, the capacitance seen at the input node of the proposed TIA circuit can be calculated as the summation of different parasitic capacitances, as in equation (7).

$$C_{in} = C_{pd} + C_{gs,MN2} + C_{gd,MN2} + C_{gs,MN1} + C_{gd,MN1} \quad (7)$$

So, the frequency of the input pole can be calculated as equation (8).

$$\omega_{p1} = \frac{g_{m,MN1} + g_{m,MN1} \cdot g_{m,MN2} \cdot r_{o,MP2}}{C_{pd} + C_{gs,MN2} + C_{gd,MN2} + C_{gs,MN1} + C_{gd,MN1}} \quad (8)$$

Hence, the -3dB frequency of the RB-TIA stage can be expressed as equation (9).

$$f_{-3dB,RGC} = \frac{g_{m,MN1} + g_{m,MN1} \cdot g_{m,MN2} \cdot r_{o,MP2}}{2\pi(C_{pd} + C_{gs,MN2} + C_{gd,MN2} + C_{gs,MN1} + C_{gd,MN1})} \quad (9)$$

Moreover, the input referred thermal noise of the active RGC stage can be written as equation (10), as follows:

$$\overline{i_{in,Noise}^2} = 4KT\gamma g_{m,MP1} + \frac{4KT}{g_{m,MN1}} \left(\gamma + \frac{1}{g_{m,MN1} \cdot r_{o,MP1}} \right) [\omega^2 \cdot C_{in}^2] \quad (10)$$

Where, γ is the noise factor, T is temperature and K is the Boltzmann constant.

So, as it can be concluded from equation (10), decreasing $g_{m,MP1}$ and increasing $g_{m,MN1}$ makes it possible to reduce the thermal noise value of the RB-TIA circuit. Furthermore, the RGC structure is followed by a common drain and common source amplifiers, which are used to provide extra gain and proper -3dB frequency for the RB-TIA circuit.

Moreover, M_6 and M_7 form an active inductive load. This active load starts to resonate with the output capacitance load and as a consequence the -3dB frequency bandwidth can be extended without the requirement of dissipating higher values of power.

Giving the above facts, the open-loop gain value for these two stages can be calculated as equations (11) to (13).

$$A_{v,Gain\ Stage} = A_{v,CD} \times A_{v,CS} \quad (11)$$

$$A_{v,CD} \approx \frac{g_{m,M4}}{g_{m,M4} + g_{mb,M4}} \quad (12)$$

$$A_{v,CS} = g_{m,M5} \cdot Z_D \quad (13)$$

Where, $A_{v,CD}$ and $A_{v,CS}$ are the voltage gain of common-drain and common source amplifiers respectively, while Z_D represents the load impedance at the drain of M_6 which is equal to equation (14).

$$Z_D = \frac{r_{o7} \cdot C_{gs6} \cdot S + 1}{g_{m6} + C_{gs6} \cdot S} \quad (14)$$

Additionally, the value of the active inductor, which resonates with the load capacitance at the output, can be extracted from equation (14), as in equation (15).

$$L = \frac{C_{gs6}}{g_{m6}} \left(r_{o7} - \frac{1}{g_{m6}} \right) \quad (15)$$

Moreover, adding R_f as a negative feedback network not only stabilizes the RB-TIA circuit but also reduces the thermal noise value of the gain stage [14]. So, by considering the feedback network, the closed-loop transimpedance gain of the gain stage can be approximated as in equation (16) as follows:

$$A_{f,Gain\ Stage} \approx R_f \quad (16)$$

Furthermore, the feedback network affects the input impedance (Z_{in}) as well as the value of the input pole frequency (ω_{-3dB}) of the gain stage. So, it can be written as equations (17) and (18), as follows:

$$Z_{in,Gain\ Stage} = \frac{R_f}{1 + A_{f,Gain\ Stage}} \quad (17)$$

$$\omega_{-3dB,gain\ stage} = \frac{1 + A_{f,Gain\ Stage}}{C_{in,Gain\ Stage} \cdot R_f} \quad (18)$$

However, due to the fact that the photodiode's input parasitic capacitance has a high value ($C_{PD} \approx 250\text{fF}$), the dominant pole is formed at the input of the RB-TIA, and the input pole of the gain stage, which is expressed in equation (18), can be neglected.

4. RECEIVER SYSTEM

In order to provide a proper gain value, three stages of differential limiting amplifiers with active loads are used after the RB-TIA as in Fig. 4, which shows the LA stage building block and the structure of each cell gain.

As it is shown in Fig. 4, each cell gain of the LA stage benefits from an active inductive peaking technique. The equivalent circuit model of each cell gain is presented in Fig. 5, in which by using half circuit technique, gain value of each cell gain can be calculated as in equation (19).

$$A_V = g_{m1} \times Z_{out,LA} \quad (19)$$

Where, $Z_{out,LA}$ is the output impedance of each cell gain expressed as equation (20) as follows:

$$Z_{out,LA} = \frac{r_{o5} \cdot C_{gs3} \cdot S + 1}{g_{m3} + C_{gs3} \cdot S} \quad (20)$$

Furthermore, cascading three cell gains of amplifiers decreases the total -3dB frequency. Assuming the transfer function of LA stage as $A_v = \frac{A_{V0} \cdot \omega_n^2}{S^2 + 2\xi \omega_n S + \omega_n^2}$, where ξ refers to the corresponding damping factor, the value of -3dB frequency for each cell gain can be written as equation (21) as follows[16]:

$$\omega_s = \left[1 - 2\xi^2 + \sqrt{(1 - 2\xi^2)^2 + 1} \right]^{\frac{1}{2}} \times \omega_n \quad (21)$$

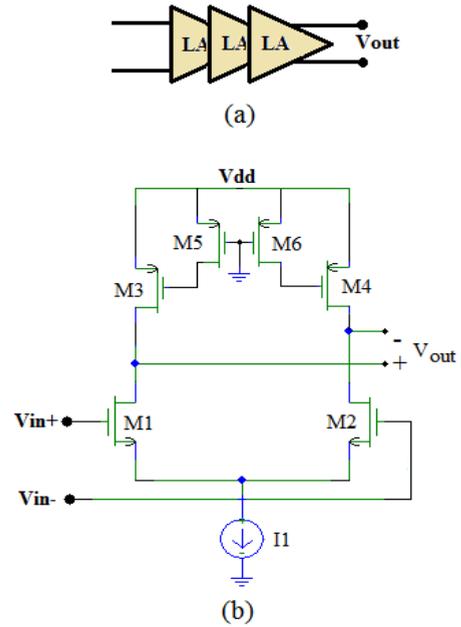


Fig. 4. Limiting amplifier (a) block diagram (b) scheme of each cell gain.

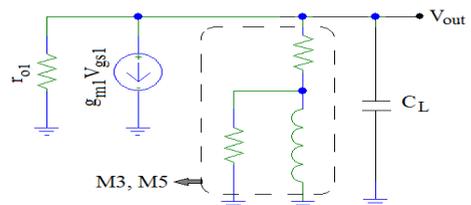


Fig. 5. Equivalent circuit model of each cell gain using half circuit technique.

Thus, the -3db frequency for three stages of LAs can be expressed as follows [17]:

$$w_c = \left[1 - 2\xi^2 + \sqrt{(1 - 2\xi^2)^2 - \left(1 - 2\frac{1}{2}\right)} \right]^{\frac{1}{3}} \times w_n \quad (22)$$

In which, ξ must be equal to $\sqrt{2}/2$, so that a flat response can be achieved.

5. SIMULATION RESULTS

The performance of the RB-TIA circuit is simulated and analyzed in HSPICE using 65nm CMOS technology BSIM4 parameters. Fig. 6 depicts the simulated frequency response of the RB-TIA. The simulation presents 46.2dBΩ transimpedance gain for the RB-TIA. As in Fig .6, a peaking occurs in the frequency response due to the implementation of the active inductor. The gain rises up to 46.55dBΩ. The -3dB frequency of the RB-TIA is equal to 3.5GHz. Also, simulations show 15pA/√Hz input referred noise for the

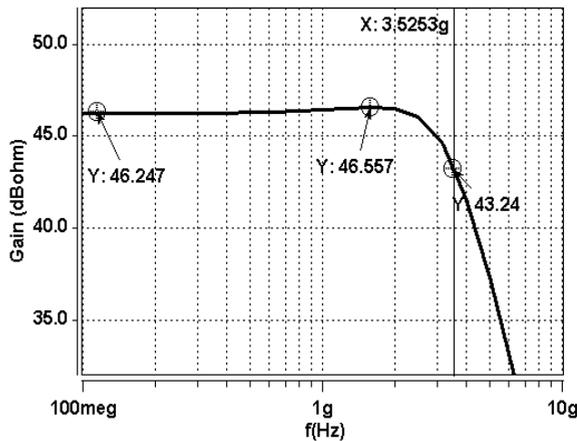


Fig. 6. RB-TIA Frequency Response.

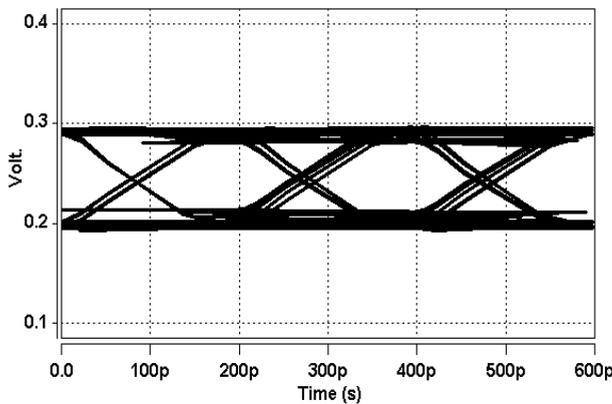


Fig. 7. Simulated eye-diagram using NRZ pseudorandom bit sequence 2²³-1 for 150µA input signal.

RB-TIA, and 573µW power consumption using 1 volt supply.

Moreover, eye-diagram of the RB-TIA is simulated in HSPICE using NRZ pseudorandom bit sequence 2²³-1 for 150µA input signal, which is shown in Fig. 7. As in this figure, the eye is vertically opened clearly (100mV).

Furthermore, the sensitivity of the frequency response of the RB-TIA vs. temperature variations is investigated and the results are shown in Fig. 8. As it can be seen for 80°C variation in temperature, the transimpedance gain varies about 1.3dB and the frequency bandwidth varies from 3.1Giga Hz to 3.7Giga Hz.

Also, Fig. 9 demonstrates the effect of V_{DD} variations on frequency response. For 1.1V_{DD}, the gain value (transimpedance gain) increases up to 48.5dBΩ, while the -3dB frequency decreases to 3GHz, and for 0.9V_{DD}, the gain value decreases to 45.8dBΩ while the -3dB frequency increases up to 3.6GHz.

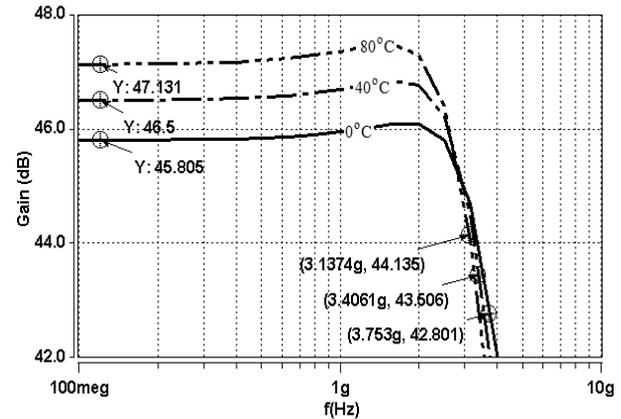


Fig. 8. Effect of temperature variation on frequency response for 80°C variation.

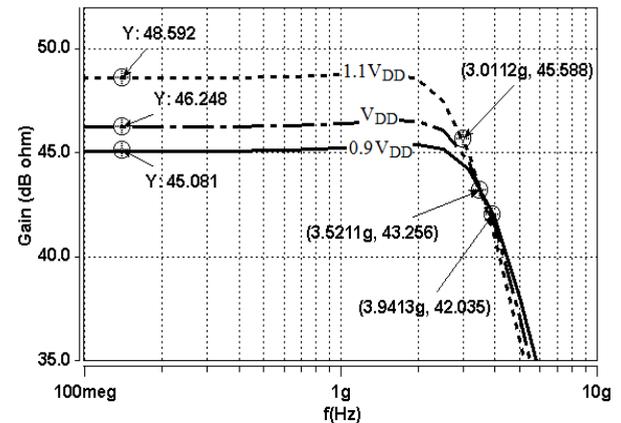


Fig. 9. Demonstration of frequency response according to variations of V_{DD}.

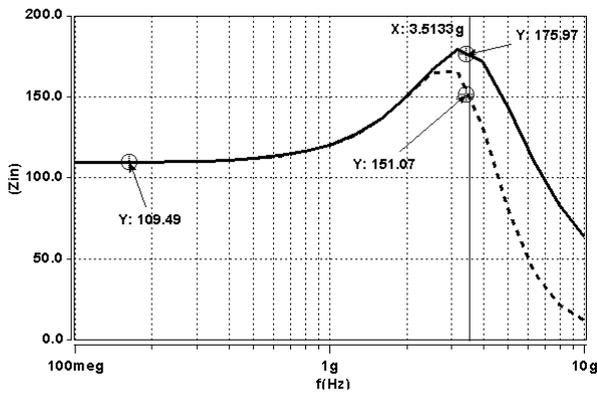


Fig. 10. Simulated input impedance (—) and input resistance (---) of the RB-TIA.

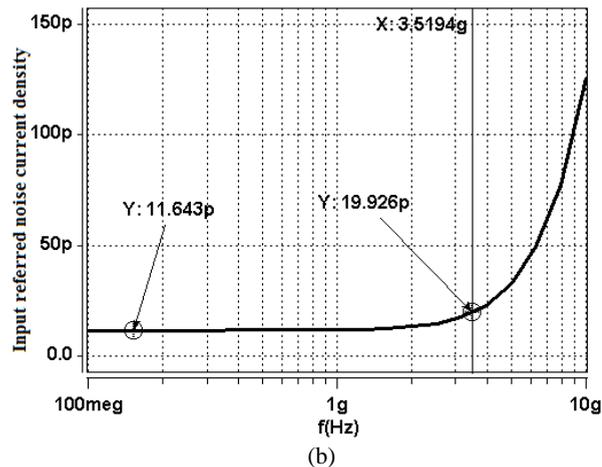
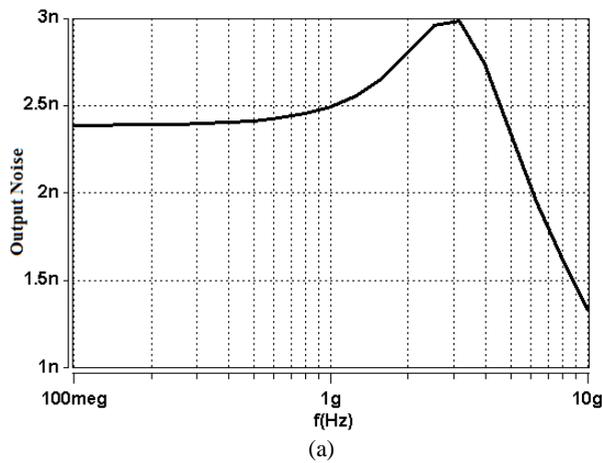


Fig. 11. (a) Output noise and (b) input referred noise of the RB-TIA.

Also, in order to analyze the input impedance/resistance of the RB-TIA, the input impedance and resistance of the RB-TIA are simulated and shown in Fig. 10. As shown in Fig. 10, at -3dB frequency the input resistance is equal to 151Ω and at low frequencies is equal to 109.5Ω , which is a low value.

Furthermore, in Fig. 11 input referred noise and output noise are shown. As shown in Fig. 11, the noise value is equal to $11.6p$ at low frequencies, while, at -3dB frequency the input referred noise is equal to $19.9p$.

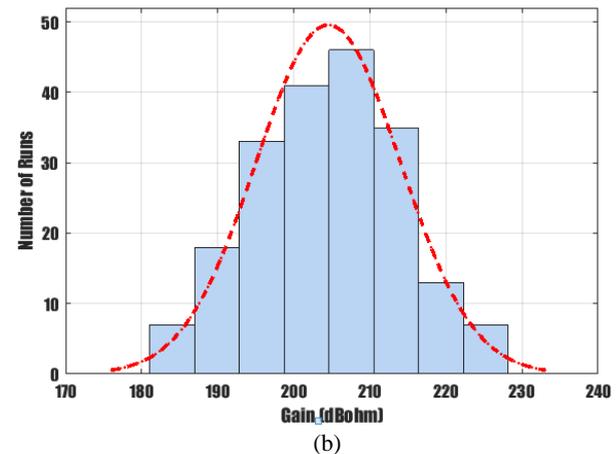
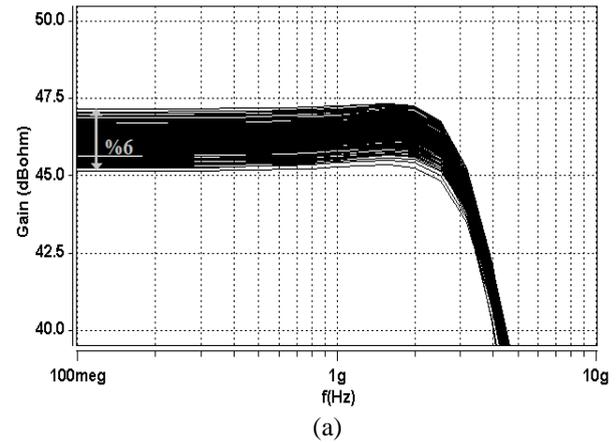


Fig. 12. MONTECARLO analysis (a) on frequency response (b) on transimpedance gain.

Moreover, analyzing the mismatch in fabrication process of the proposed RB-TIA is of interest. So, MONTECARLO analysis is done on frequency response and is shown in Fig. 12a, while, Fig. 12b shows MONTECARLO analysis specifically on the value of transimpedance gain, which presents the mean value of 204.5Ω and standard deviation of 9.5Ω .

Moreover, the effect of width variations of MN1 and MN2 on input resistance of the RB-TIA circuit, according to equations (5) and (6), is summarized in Table 1 and Table 2 and shown in Fig. 13. As it is obvious in Fig. 13, increasing the width of MN1 and MN2 results in reduction in the value of input resistance of the proposed TIA circuit.

Furthermore, the effect of width variations of MP1 on the level of input referred white noise of the RB-TIA circuit, according to equation (10), is summarized in

Table 2 and shown in Fig. 14. As it is obvious in Fig. 14, increasing the width of MP1 results in an increase

in the level of white noise (input referred) of the RB-TIA circuit.

Table 1. Relation of width of MN1 with input resistance of the RB-TIA.

W_{MN1}	200nm	400nm	600nm	800nm	1 μ m	1.5 μ m	2 μ m	2.5 μ m
R_{in}	1640 Ω	590 Ω	379 Ω	294 Ω	249 Ω	194 Ω	169 Ω	154 Ω

Table 2. Relation of width of MN2 with input resistance of the RB-TIA.

W_{MN2}	200nm	400nm	600nm	800nm	1 μ m	1.5 μ m	2 μ m	2.5 μ m
R_{in}	487 Ω	376 Ω	308 Ω	265 Ω	236 Ω	194 Ω	172 Ω	158 Ω

Table 3: Relation of width of MP1 with level of input referred white noise of the RB-TIA.

W_{MP1}	200nm	500nm	750nm	1 μ m	1.5 μ m	2 μ m	2.5 μ m
Input referred white noise	1.3p	5p	6.7p	8p	9.9p	11.3p	12.3p

Moreover, the whole optical receiver system is simulated in HSPICE. Fig. 15 shows the simulated frequency response of the complete receiver system, which shows 80dB (10⁷000) gain value and 3.5Giga Hz frequency bandwidth. Also, power dissipation for two stages of the RB-TIA (including the main RB-TIA and the TIA replica) and three stages of LA cells is equal to 4.76mW using 1V supply.

Furthermore, Table 4 summarizes the properties of the proposed RB-TIA and the LA stage.

Additionally, Table 5 compares the proposed RB-TIA with other works. In the RB-TIA, a smaller CMOS technology is used. So, a smaller supply voltage is required. As it can be seen in Table 5, the power consumption of the RB-TIA is much less than other reported designs. In comparison with [18], the power consumption of the proposed TIA is about one-tenth of what it is reported in [18].

Table 4. Properties of the RB-TIA and the LA stages.

	TIA	LA
Gain	46.24dB Ω	33.7dB
Bandwidth	3.52GHz	3.9GHz
Power Consumption	573 μ W	3.6mW
Supply Voltage	1V	1V

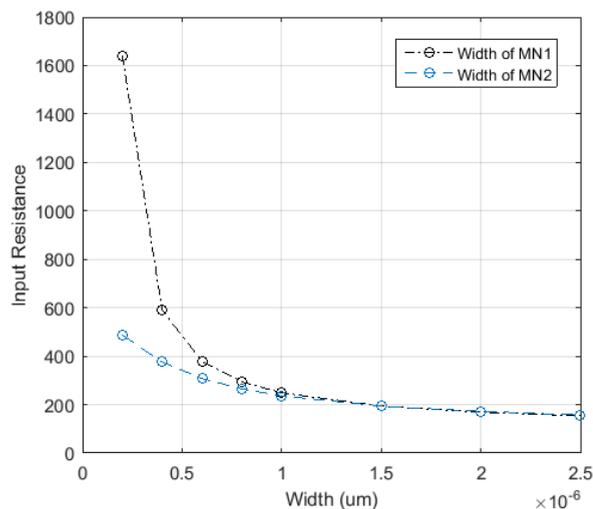


Fig. 13. Relation of width of MN1 and MN2 on input resistance of the RB-TIA.

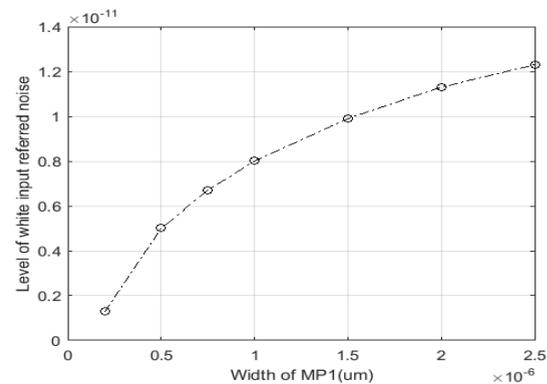


Fig. 14. Relation of width of MP1 on level of input referred white noise of the RB-TIA.

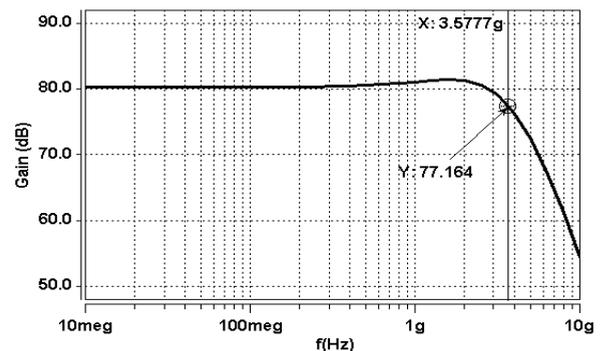


Fig. 15. Frequency response of the optical front-end.

Moreover, Table 6 compares the proposed optical receiver with other reported optical receivers. Figure of Merits (FOM) as a standard definition for a comprehensive comparison among the proposed regulated based circuit and other designs, used in Tables 5 and 6, are defined as follows:

$$FOM1 = \frac{Gain \times BW}{P_{DC}} \left(\frac{\Omega.GHz}{mW} \right) \quad (23)$$

$$FOM2 = \frac{Gain \times BW \times C_{in}}{P_{DC} \times In.Ref.Noise} \left(\frac{\Omega.GHz.pF}{mW.(pA/\sqrt{Hz})} \right) \quad (24)$$

Table 5. Comparison of the presented RB-TIA with some other designs.

	[15]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	This Work
Year	2011	2016	2013	2015	2016	2016	2016	2017	2017	2017
Technology (CMOS)	0.35 μ m	0.18 μ m	0.18 μ m	0.13 μ m	0.13 μ m	0.13 μ m SiGe BiCMOS	0.18 μ m	0.18 μ m	0.13 μ m SiGe BiCMOS	65nm
Gain(dB Ω)	54.2	55-69	46	50.1	54	72	58	59	83.7	46.24
Bandwidth (GHz)	2.3	1	8	7	11.5	38.4	8.1	7.9	32.1	3.52
C _{pd} (fF)	500	-	250	250	-	-	300	300	-	250
Power Consumption (W)	58m	6m	31.5m	7.5m	45m	261m	34.8m	18m	150m	573 μ
Supply Voltage (V)	3.3	1.8	1.8	1.5	1.5	3.3	1.8	1.8	3.3	1
Input referred noise(pA/ \sqrt Hz)	18.8	9.33	40	31.3	6.8	14.8	15	23	-	15
Number of inductors	0	0	2	0	2	0	2	2	0	0
FoM1	20	417	50.6	299	128	585	184.8	425	3276	1261
FoM2	0.53	0.31	2.4	-	-	3.69	5.54	-	-	21

Table 6. A comparison among the proposed optical receiver and other optical receivers.

	Gain	Bandwidth / Data Rate	C _{pd}	Power Consumption	Supply Voltage	FOM1
[28]	87dB	1.4GHz	2pF	50mW	1.8V	626
[29]	60.4dB	2.5GHz	0.5pF	35.3mW	1.1V	74
[30]	78dB	1GHz	1.8pF	12mW	1V	662
[31]	110dB	2.5Gb/s	-	138mw	1.8V/3.3V	-
[32]	92dB	3.125Gb/s	-	46.3mW	1.2V	-
[33]	78.5dB	3.125Gb/s	-	50mW	1.2V	-
This work	80dB	3.5GHz	0.25pF	4.76mW	1V	7352

6. CONCLUSIONS

A low-power optical receiver system operating at 5Gb/s is presented, which employs a low-input-resistance transimpedance amplifier and three stages of active differential limiting amplifiers. In order to extend the bandwidth, an active RGC stage, which benefits from a low input resistance, is used as the input stage of

the TIA, and in order to obtain proper transimpedance gain, a gain stage is used after the RGC stage, which uses an active inductive peaking technique. Such a combination results in a low-power consumption circuit as the RB-TIA. Moreover, each cell gain of the differential LA stage benefits from active inductive peaking technique, which provides proper gain, while

consumes low power. Simulations in HSPICE using 65nm CMOS technology parameters for the TIA show 3.52GHz frequency bandwidth, $951.8nA_{rms}$ input referred noise, $46.24dB\Omega$ gain, and only $573\mu W$ power consumption, while, simulations for the optical receiver show 3.5GHz frequency bandwidth, $80dB\Omega$ gain, and $4.76mW$ power consumption using 1V supply. Discussions and analysis indicate that the proposed receiver is suitable to work as a low-power, 5Gbps optical receiver.

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